PATENT ABSTRACTS OF JAPAN

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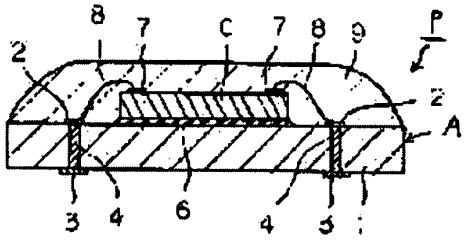
(71)Applicant : KYOCERA CORP
(72)Inventor : YONEKURA HIDETO
AZUMA MASAHIKO
HAMADA NORIAKI

(54) SEMICONDUCTOR ELEMENT MOUNTING WIRING SUBSTRATE AND WIRING SUBSTRATE MOUNTING STRUCTURE

(57)Abstract:
PROBLEM TO BE SOLVED: To provide a semiconductor element mounting wiring substrate in which no cracks occur in a sealer, and this causes to achieve sufficient sealing performance, and conductivity in connection is increased.



SOLUTION: In this substrate P, a metallized wiring layer 2 is arranged on a surface and an interior of an insulation substrate 1 of which a coefficient of thermal expansion at 40 to 400°C is prescribed to be 8 to 25 ppm/°C, and a semiconductor element C is mounted on this BGA semiconductor element accommodating package A. The metallized wiring layer 2 of the BGA semiconductor element accommodating package A is connected to an element 7 for connecting the semiconductor element C by use of a bonding wire 8. A filler is mixed with a thermosetting resin, and the semiconductor element C and the bonding wire 8 are sealed with a sealer 9 prescribed so that the coefficient of thermal expansion at 40 to 400°C is 8 to 25 ppm/°C, and the Young's modulus is 30 GPa or less.

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PROBLEM TO BE SOLVED: To provide a semiconductor element mounting wiring substrate in which no cracks occur in a sealer, and this causes to achieve sufficient sealing performance, and conductivity in connection is increased.

SOLUTION: In this substrate P, a metallized wiring layer 2 is arranged on a surface and an interior of an insulation substrate 1 of which a coefficient of thermal expansion at 40 to 400°C is prescribed to be 8 to 25 ppm/°C, and a semiconductor element C is mounted on this BGA semiconductor element

accommodating package A. The metallized wiring layer 2 of the BGA semiconductor element accommodating package A is connected to an element 7 for connecting the semiconductor element C by use of a bonding wire 8. A filler is mixed with a thermosetting resin, and the semiconductor element C and the bonding wire 8 are sealed with a sealer 9 prescribed so that the coefficient of thermal expansion at 40 to 400°C is 8 to 25 ppm/°C, and the Young's modulus is 30 GPa or less.

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* NOTICES *

CLAIMS

[Claim(s)]

[Claim 1] On the wiring substrate with which the coefficient of thermal expansion in 40-400 degrees C comes to arrange a metallizing wiring layer in the front face and the interior of an insulating substrate which were specified [degree C] in 8-25 ppm / Lay a semiconductor device and the electrode for connection of the metallizing wiring layer of this wiring substrate and a semiconductor device is connected using a bonding wire. The wiring substrate for semiconductor device mounting which made said semiconductor device and bonding wire close with the encapsulant which mixed the filler to thermosetting resin, specified the coefficient of thermal expansion in 40-400 degrees C to it in 8-25 ppm/degree C, and specified Young's modulus to 30 or less GPas.

[Claim 2] Wiring substrate mounting structure where the wiring substrate for semiconductor device mounting of claim 1 was formed on the external electrode circuit board.

[Translation done.]

* NOTICES *

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DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Field of the Invention] This invention relates to the wiring substrate for semiconductor device mounting, After using a bonding wire and connecting a semiconductor device on the wiring substrate of a surface mount mold especially, it is related with the wiring substrate for semiconductor device mounting excellent in the heat history property, endurance, and dependability which closed the semiconductor device and the bonding wire using the encapsulant which consists of thermosetting resin, and were made to paste up. It is related with the wiring substrate mounting structure where the semiconductor device mounting wiring substrate of this invention which furthermore starts was formed on the external electrode circuit board.

[0002]

[Description of the Prior Art] A wiring substrate arranges a metallizing wiring layer in the front face or the interior of an insulating substrate, and has a package for semiconductor device receipt for laying semiconductor integrated circuit components, such as a semiconductor device, especially LSI (large-scale-integrated-circuit component), as an example of representation.

[0003] According to this package for semiconductor device receipt (the package for semiconductor device receipt is hereafter written as a package), two or more metallizing wiring layers which consist of refractory metal powder, such as a tungsten and molybdenum, are arranged in the front face and the interior of an insulating substrate which consist of alumina ceramics, and the so-called

wirebonding method which connects electrically through a wire to the semiconductor device laid in the top face of an insulating substrate is adopted. The semiconductor device and the bonding wire are closed with the encapsulant which furthermore consists of thermosetting resin.

[0004] According to the package of such structure, if the degree of integration of a semiconductor device becomes high, the number of electrodes formed in a semiconductor device will increase, and the number of terminals in a wiring substrate will also increase in connection with this.

[0005]

[Problem(s) to be Solved by the Invention] the case where it is used as a wiring substrate for semiconductor device mounting for mounting the above-mentioned package on the external electrode circuit board -- the connection terminal of a wiring substrate, and wiring of the external electrode circuit board -- although a conductor is connected electrically, the external electrode circuit board usually consists of printed circuit boards which consisted of composites of the organic ingredient or organic ingredient containing a resinous principle, and a minerals ingredient. On the other hand, ceramics, such as an alumina and a mullite, constitutes the insulating substrate of a package, it has the high intensity of 200 or more MPas, and, moreover, high dependability is acquired by using multilayering techniques, such as a metallizing wiring layer.

[0006] In the wiring substrate for semiconductor device mounting of such a configuration, repeat impression of the heat emitted at the time of actuation of a semiconductor device was carried out to the both sides of an insulating substrate and an external electrical circuit substrate, and, thereby, the distortion by thermal stress had occurred between connections. Incidentally, the coefficient-of-thermal-expansion difference of an insulating substrate and an external electrical circuit substrate is 10 ppm/degree C or more.

[0007] When less than 300-piece extent has comparatively few connection terminals prepared in the package Although the effect by thermal stress is small, if a connection terminal becomes large-sized to extent which becomes 300 or

more pieces, thermal stress will also increase. The sake, Stress concentrates on a junction interface with a conductor. the cycle of actuation/halt of a semiconductor device -- wiring of the periphery section of the connection terminal of a package and this connection terminal, and an external electrical circuit substrate -- that a connection terminal exfoliates from an insulating substrate **** -- a connection terminal -- wiring of an external electrical circuit substrate -- from a conductor -- exfoliating -- consequently, the connection terminal of a package -- wiring of an external electrode circuit -- the technical problem that electrical installation could not be stabilized and carried out to a conductor over a long period of time occurred.

[0008] In order to cancel this technical problem, replacing with ceramics, such as an alumina and a mullite, and using high temperature expansion coefficient crystallized glass with a more large coefficient of thermal expansion etc. for the component of the insulating substrate of a package is examined (refer to JP,8-279574,A and JP,10-167822,A).

[0009] Although the coefficient of thermal expansion was 8-25 ppm/degree C, this high temperature expansion coefficient crystallized glass had it compared with alumina ceramics and the faulty connection who arises between the connections between a package and an external electrical circuit substrate has avoided, [fairly high] By on the other hand using such high temperature expansion coefficient crystallized glass Semiconductor device which consists of silicon (coefficient of thermal expansion : 2-3 ppm/(degree C)) A differential thermal expansion becomes large. By this The metallizing wiring layer of a wiring substrate and the electrode for connection of a semiconductor device are connected using a bonding wire. When the package (insulating substrate) which furthermore comes to close a semiconductor device and a bonding wire using the encapsulant containing thermosetting resin is mounted in the external electrode circuit board, Stress concentrated between encapsulant and the top-face corner section of a semiconductor device, the crack occurred in encapsulant, and sufficient closure was not made, consequently the technical problem that

connection resistance deteriorated in reliability trials, such as a high-humidity/temperature trial, (electric resistance becomes high) arose.

[0010] Therefore, the result of having repeated research wholeheartedly so that this invention persons might make the thermal stress produced in an insulating substrate, a semiconductor device, and encapsulant easing in view of the above-mentioned situation, As opposed to the insulating substrate as which the coefficient of thermal expansion was specified [degree C] in 8-25 ppm /the coefficient of thermal expansion after hardening (40-400 degrees C) in 8-25 ppm /[degree C] It found out that this thermal stress was absorbed and the effect became small notably by covering encapsulant of an ingredient presentation with which Young's modulus (40-400 degrees C) is specified to 30 or less GPas.

[0011] this invention is completed by the above-mentioned knowledge, the purpose is that a crack does not occur in a wiring substrate and the encapsulants which were boiled and were covered to the semiconductor device, such as a package, sufficient closure engine performance is attained, and it is in offering the wiring substrate for semiconductor device mounting which raised the energization nature in connection.

[0012] Other purposes of this invention are to offer the wiring substrate mounting structure which carried out the surface mount of the wiring substrates, such as a package, to the external electrical circuit substrate where faced, made it stabilize and connect firmly over a long period of time, and this attained dependability over a long period of time.

[0013]

[Means for Solving the Problem] The wiring substrate for semiconductor device mounting of this invention on the wiring substrate with which the coefficient of thermal expansion in 40-400 degrees C comes to arrange a metallizing wiring layer in the front face and the interior of an insulating substrate which were specified [degree C] in 8-25 ppm / Lay a semiconductor device and the electrode for connection of the metallizing wiring layer of this wiring substrate and a semiconductor device is connected using a bonding wire. It is characterized by

making a semiconductor device and a bonding wire close with the encapsulant which mixed the filler to thermosetting resin, specified the coefficient of thermal expansion in 40-400 degrees C to it in 8-25 ppm/degree C, and specified Young's modulus to 30 or less GPas.

[0014] Wiring substrate mounting structure of this invention is characterized by forming the wiring substrate for semiconductor device mounting of this this invention on the external electrode circuit board.

[0015]

[Embodiment of the Invention] Hereafter, drawing explains this invention to a detail. Drawing 1 is the sectional view of the wiring substrate P for semiconductor device mounting which mounted the semiconductor device in the package A for BGA mold semiconductor device receipt (the following, Package A) which is said wiring substrate. Drawing 2 is the sectional view of the wiring substrate mounting structure S where the wiring substrate P for semiconductor device mounting was mounted in the external electrical circuit substrate B (the following, the circuit board B).

[0016] As shown in drawing 1 , the wiring substrate P for semiconductor device mounting mounts a semiconductor device C in Package A, the metallizing wiring layer 2 connected with a semiconductor device C is formed in the front face of an insulating substrate 1 in this package A, and the connection pad 3 is attached. the metallizing wiring layer 2 -- a beer hall -- it connects with the connection pad 3 electrically through the conductor 4.

[0017] Adhesion immobilization of the semiconductor device C is carried out to the glue line 6 which consists of a silicon (Si) ingredient, for example, consists of thermosetting resin being on the front face of an insulating substrate 1. When a novolak mold epoxy resin and the bisphenol A mold epoxy resin are used for this thermosetting resin, it is good at the point of excelling in an adhesive property with an insulating substrate 1. Moreover, the electrode 7 for connection is formed in a semiconductor device C, and the bonding wire 8 connects with the metallizing wiring layer 2 electrically. Furthermore, the closure is carried out to

encapsulant 9 being about a semiconductor device C and a bonding wire 8.

[0018] After applying die attachment resin to insulating-substrate 1 front face for mounting a semiconductor device C in Package A, lay a semiconductor device C and it is made to harden at the temperature of about 100-200 degrees C, the metallizing wiring layer 2 on an insulating substrate 1 is further connected with a semiconductor device C by the bonding wire 8, and after covering that thermosetting resin is also about a semiconductor device C and a bonding wire 8 and closing, it is made to harden at the temperature of about 100-200 degrees C, and makes with encapsulant 9.

[0019] As shown in drawing 2 , the wiring substrate P for semiconductor device mounting of the above-mentioned configuration is mounted in the circuit board B through the connection terminal 5, and it considers as the wiring substrate mounting structure S. The connection terminal 5 is constituted by the ball-like solder ball, and is attached with solder etc. to the connection pad 3.

[0020] The circuit board B makes an insulating base 10 a subject, and an insulating base 10 consists of a glass-epoxy resin, glass-polyimide resin composite material, etc. which contain glass etc. as a filler component to an epoxy resin, phenol resin, aramid resin, polyimide resin, and at least one sort of thermosetting resin chosen from polyolefin resin. Covering formation is carried out and the wiring layer 11 containing at least one sort of metals chosen as the front face of this insulating base 10 from Cu, Au, aluminum, nickel, and Pb-Sn is equivalent to a printed circuit board etc.

[0021] Next, an insulating substrate 1 and encapsulant 9 are explained in full detail.

It is good to make ingredient selection from the ceramics so that the coefficient of thermal expansion in 140-400 degrees C of insulating substrates may be specified [degree C] in 8-25 ppm /, and the Young's modulus in 40-400 degrees C constitutes 200 or less GPas by the ceramic material of 150 or less GPas suitably desirably.

[0022] glass components, such as lithium silicic acid system glass which is

indicated by the detail in the letter of JP,10-167822,A as an ingredient of such a property, PbO system glass, ZnO system glass, and BaO system glass, -- receiving -- ENSUTE tightness, forsterite, and SiO2 Various ceramic fillers, such as a system filler, MgO and ZrO2, and petalite, are mixed, and there are some which were subsequently calcinated.

[0023] It is the rate of 20 - 80 volume % about the glass which contains BaO five to 40% of the weight suitably among these ceramic fillers, and the sintered compact which calcinated the Plastic solid which contains Quartz at a rate of 80 - 20 volume %, and was obtained is good. The sintered compact which permuted some Quartz by the zirconia and was obtained from a chemical-resistant viewpoint of a sintered compact still more suitably is desirable.

[0024] If it is this sintered compact, it can calcinate to the metallizing wiring layer and coincidence which it can manufacture easily that it is also at good repeatability about the product of homogeneity, and a surrendering point becomes comparatively low, and low-temperature baking can do the addition of a glass component at least by this by in addition containing BaO five to 40% of the weight for a glass component, consequently consist of Cu, Ag, etc.

[0025] Since a glass content can be reduce , the amount of fillers can be increase in connection with this and burning shrinkage initiation temperature can moreover also be raise because the surrender point of BaO system glass furthermore become low even at 400-800 degrees C , binders for shaping , such as organic resin added at the time of shaping , can be remove efficiently , and baking conditions with the metallized layer by which coincidence baking be carry out with an insulator can be match . Thus, when specifying the surrendering point of BaO system glass, it is good to make it a presentation to which the surrendering point becomes within the limits which is 400-650 degrees C.

[0026] Encapsulant 9 encapsulant 9 mixes a filler to thermosetting resin, adjusts the mixed state, and if the coefficient of thermal expansion in 40-400 degrees C sets in 8-25 ppm/degree C in after hardening and Young's modulus is set to 30 or less GPas, it has various presentations.

[0027] In this thermosetting resin, it is phenol resin Urea resin Melamine resin Epoxy resin Unsaturated polyester resin Diallyl phthalate resin Polyimide resin Silicone resin There is polyurethane resin etc. and it is a bisphenol system epoxy resin above all, Phenol novolak system epoxy resin, Cresol novolak system epoxy resin, Bromine-ized epoxy resin, Epoxy resins, such as cycloaliphatic epoxy resin, are desirable. Moreover, in order to control the Young's modulus and the coefficient of thermal expansion of encapsulant in the aforementioned range, to thermosetting resin, to said thermosetting resin 100 weight section, minerals, such as quartz glass, an alumina, a mica, zirconium silica KETO, and lithium silicate, are blended as the 100 - 150 weight section is also, and are adjusted.

[0028] thus, the coefficient of thermal expansion of the encapsulant 9 after thermosetting resin hardens by adjusting a presentation -- 8-25 ppm/degree C -- and Young's modulus is set to 30 or less GPas.

[0029] If a coefficient of thermal expansion becomes [degree C] in less than 8 ppm /, the amount of fillers will increase, therefore the fluidity of resin will become low, mounting effectiveness will fall, and the adhesive strength to an insulating substrate 1 will decline further. Moreover, if degree C is exceeded in 25 ppm /, the thermal expansion during the time of an elevated temperature and low temperature and the difference of a heat shrink will become large, stress concentrates between encapsulant 9 and the top-face corner section of a semiconductor device C, and a crack occurs in encapsulant 9. It is good to carry out [degree C] a coefficient of thermal expansion in 8-20 ppm /desirably.

[0030] Moreover, it is suitably good for 30 or less GPas to make it 25 or less GPas, when Young's modulus exceeds 30GPa(s), deformation is small, stress concentrates between encapsulant 9 and the top-face corner section of a semiconductor device C, and a crack generates the Young's modulus of encapsulant 9 in encapsulant 9.

[0031] In this way, according to the wiring substrate P for semiconductor device mounting of this invention, desirably [ppm / (40-400 degrees C) / // 8-25 / degree

C], while specifying Young's modulus to 200 or less (40-400 degrees C) GPas, the coefficient of thermal expansion of an insulating substrate 1 By specifying the coefficient of thermal expansion of encapsulant 9 in 8-25 ppm (40-400 degrees C)/degree C, and specifying Young's modulus to 30 or less GPas While the thermal stress resulting from a semiconductor device C etc. is absorbed by the deflection of an insulating substrate 1 By bringing the coefficient of thermal expansion of the both sides of an insulating substrate 1 and the thermosetting resin (potting resin) of encapsulant 9 close The stress which curvature does not generate in a substrate and is generated in a connection with the circuit board B can be reduced. Concentration of the stress generated between encapsulant 9 and the top-face corner section of a semiconductor device C is avoided, consequently a crack stops occurring in encapsulant 9, a semiconductor device C and a bonding wire 8 are protected, and high dependability is attained to long-term use.

[0032]

[Example] Three kinds of ceramics (insulating-substrate material A, B, and C) was prepared as shown in Table 1, and the sintered compact with a configuration of 5x4x40mm was produced as each ceramic ingredient is also.

[0033]

[Table 1]

絶縁基板材	ガラス成分		フィラー成分	
	組成 ( ) 内は重量%	体積 %	組成	体積 %
A	SiO_2(78)-Li_2O(10)-Al_2O_3(4)-K_2O(4)-P_2O_5(2)-Na_2O(2)	50	フォルステライト	50
B	SiO_2(78)-Li_2O(10)-Al_2O_3(4)-K_2O(4)-P_2O_5(2)-Na_2O(2)	35	フォルステライト クオーツ	30 35
C	SiO_2(45)-Al_2O_3(6)-B_2O_3(9)-CaO(5)-BaO(37)	50	クオーツ	50

[0034] Subsequently, when Young's modulus and the coefficient of thermal expansion in 40-400 degrees C were measured about each sintered compact, the result as shown in Table 2 was obtained.

[0035]

[Table 2]

絶縁基板材	ヤング率 (GPa)	熱膨張係数 (ppm/℃)
A	108	11.7
B	114	14.6
C	80	12.2

[0036] Moreover, the insulating substrate 1 with a thickness of 0.4mm was produced using each insulating-substrate material A, B, and C. At that time, the metallizing wiring layer and through hole which use copper as a principal component were formed, and the connection pad which consists of much Cu metallizing was formed in the part linked to the through hole on the top face of a substrate.

[0037] Subsequently, the semiconductor device C (the coefficient of thermal expansion in 40-400 degrees C : 2.6 ppm/(degree C)) which consists of Si was pasted up in 1-hour atmospheric air at 150 degrees C using die attachment resin. Then, the metallizing wiring layer 2 on an insulating substrate 1 was connected with the semiconductor device C by the bonding wire 8.

[0038] After an appropriate time, in the various insulating substrates 1 which consist of insulating-substrate material A, B, and C, covered various sealing agents as further shown in Table 3 and 4 on a semiconductor device C and a bonding wire 8, and had by whenever [stoving temperature / of 180 degrees C], it was made to harden in 2-hour atmospheric air, and the various wiring substrates P for semiconductor device mounting of sample No.1- sample No.24 were produced.

[0039] As shown in these tables, the phenol novolak mold epoxy resin and the cresol novolak mold epoxy resin were used as heat-curing mold resin of a sealing agent, quartz glass and an alumina were added as a filler to it, and the thing kneaded and prepared was used.

[0040]

[Table 3]

試料No	絶縁基板材料	封止剤の組成	
		樹脂の種類	石英ガラス（重量部）
1	A	フェノールノボラック型エポキシ樹脂	50
2			100
3			110
4			130
5			150
6			200
7	B	クレゾールノボラック型エポキシ樹脂	50
8			100
9			110
10			130
11			150
12			200

[0041]

[Table 4]

試料No	絶縁基板材料	封止剤の組成	
		樹脂の種類	アルミナ（重量部）
13	C	フェノールノボラック型エポキシ樹脂	50
14			100
15			110
16			130
17			150
18			200
19	A	クレゾールノボラック型エポキシ樹脂	50
20			100
21			110
22			130
23			150
24			200

[0042] Moreover, the coefficient of thermal expansion and Young's modulus of a

sealing agent which are used for the wiring substrate P for these semiconductor device mounting are shown in Table 5 and Table 6.

[0043]

[Table 5]

試料No	熱膨張係数 (ppm/℃)	ヤング率 (GPa)	TCT (回)
1	62	8.6	800
2	35	15.4	900
3	32	16.6	950
4	25	21.4	>1000
5	18	27.4	>1000
6	12	33.4	900
7	43	7.2	900
8	32	9.3	925
9	30	20.5	950
10	20	24.5	>1000
11	8	29.7	>1000
12	4	34.9	900

[0044]

[Table 6]

試料No	熱膨張係数 (ppm/℃)	ヤング率 (GPa)	TCT (回)
13	63	9.1	850
14	47	16.3	900
15	45	17.5	900
16	36	22.4	900
17	25	28.3	>1000
18	13	42.3	850
19	50	13.6	900
20	23	22.5	>1000
21	21	23.4	>1000
22	17	26.8	>1000
23	12	31.3	950
24	7	36.6	900

[0045] It asked for these coefficients of thermal expansion alpha and Young's modulus E as follows. 150 degrees C, resin is held for 1 hour and hardened -- making -- and the coefficient of thermal expansion alpha -- TMA -- law (sample size: 3.5x3.5x15mm) -- it is -- Young's modulus E -- DHA -- it asked by law (sample size: 5x0.5x50mm).

[0046] About the wiring substrate P for semiconductor device mounting of sample No.1- sample No.24 obtained in this way, when the thermal cycling test was performed, the result as shown in Table 5 and Table 6 was obtained.

[0047] about the thermal cycling test, the test sample (the wiring substrate P for semiconductor device mounting) was held every [during 15 minutes], respectively in the thermostat controlled in each temperature of -40 degrees C and 125 degrees C, this was made into 1 cycle, and this cycle was repeated a maximum of 1000 times. And the number of cycles until it checks the peeling condition within each encapsulant and peeling occurs about a semiconductor device and a bonding wire for every cycle was counted.

[0048] Peeling of the encapsulant with which the coefficient of thermal expansion of encapsulant closed the semiconductor device and the bonding wire in the ingredient whose Young's modulus is 30 or less GPas in 8-25 ppm/degree C, sample No.4, and 5, 10, 11, 17, 20-22 on the wiring substrate was not seen at all to 1000 heat cycles, but has maintained the very stable and good closure condition so that more clearly than these tables. In sample No.1-3 outside the above-mentioned range, 6-9, 12-16, and 18, 19, 23 and 24, it turned out that peeling of encapsulant occurs in less than 1000 cycles, and the dependability after mounting is missing.

[0049]

[Effect of the Invention] According to the wiring substrate for semiconductor device mounting of this invention the above passage, on the wiring substrate with which the coefficient of thermal expansion in 40-400 degrees C comes to arrange a metallizing wiring layer in the front face and the interior of an insulating

substrate which were specified [degree C] in 8-25 ppm / By having closed with the encapsulant which laid the semiconductor device, mixed the filler to thermosetting resin further, specified the coefficient of thermal expansion in 40-400 degrees C to it in 8-25 ppm/degree C, and specified Young's modulus to 30 or less GPas The wiring substrate for semiconductor device mounting which a crack stops having occurred in the encapsulant, and sufficient closure engine performance was attained by this, consequently raised the energization nature in connection has been offered.

[0050] Moreover, in the wiring substrate mounting structure of this invention, it was having carried out the surface mount of the wiring substrate for semiconductor device mounting of this this invention on the external electrode circuit board, and it could stabilize and connect firmly over the long period of time, and the wiring substrate mounting structure where this attained dependability over a long period of time has been offered.

[Translation done.]

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] It is the sectional view of the wiring substrate for semiconductor

device mounting of this invention.

[Drawing 2] It is the sectional view of the wiring substrate mounting structure of this invention.

[Description of Notations]

A The package for BGA mold semiconductor device receipt

B External electrical circuit substrate B

S Wiring substrate mounting structure

P The wiring substrate for semiconductor device mounting

C Semiconductor device

1 Insulating Substrate

2 Metallizing Wiring Layer

3 Connection Pad

4 Beer Hall -- Conductor

5 Connection Terminal

6 Glue Line

7 Electrode for Connection

8 Bonding Wire

9 Encapsulant

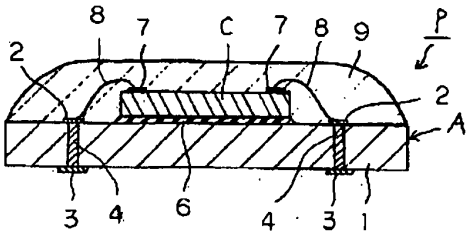
10 Insulating Base

11 Wiring Layer

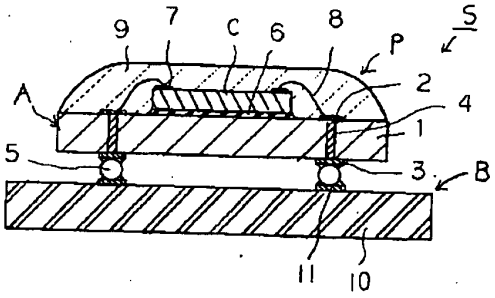
[Translation done.]

DRAWINGS

[Drawing 1]



[Drawing 2]



[Translation done.]

(19)日本国特許庁(JP)　(12)公開特許公報（A）　(11)特許出願公開番号

特開２００１－１５６４９

（Ｐ２００１－１５６４９Ａ）

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(71)出願人　000006633
京セラ株式会社
京都府京都市伏見区竹田鳥羽殿町6番地

(72)発明者　米倉　秀人
鹿児島県国分市山下町1番4号　京セラ株式会社総合研究所内

(72)発明者　東　昌彦
鹿児島県国分市山下町1番4号　京セラ株式会社総合研究所内

(72)発明者　浜田　紀彰
鹿児島県国分市山下町1番4号　京セラ株式会社総合研究所内

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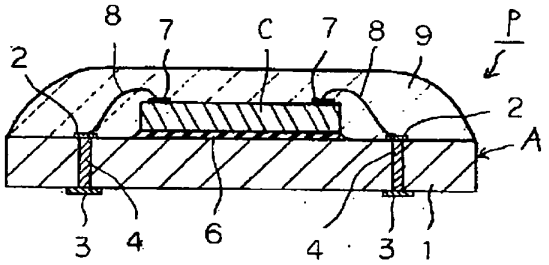
(54)【発明の名称】半導体素子実装用配線基板および配線基板実装構造

(57)【要約】

【課題】封止剤にクラックが発生しないことで、十分な封止性能を達成し、接続における通電性を高めた半導体素子実装用配線基板を提供する。

【解決手段】４０～４００℃における熱膨張係数が８～２５ｐｐｍ／℃に規定された絶縁基板１の表面および内部にメタライズ配線層２を配設してなるＢＧＡ型半導体素子収納用パッケージＡ上に、半導体素子Ｃを載置し、ＢＧＡ型半導体素子収納用パッケージＡのメタライズ配線層２および半導体素子Ｃの接続用電極７とをボンディングワイヤ８を用いて接続し、熱硬化性樹脂にフィラーを混合して４０～４００℃における熱膨張係数を８～２５ｐｐｍ／℃に、ヤング率を３０ＧＰａ以下に規定した封止剤９により半導体素子Ｃとボンディングワイヤ８とを封止せしめた半導体素子実装用配線基板Ｐ。



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【特許請求の範囲】

【請求項１】４０～４００℃における熱膨張係数が８～２５ｐｐｍ／℃に規定された絶縁基板の表面および内部にメタライズ配線層を配設してなる配線基板上に、半導体素子を載置し、該配線基板のメタライズ配線層および半導体素子の接続用電極とをボンディングワイヤを用いて接続し、熱硬化性樹脂にフィラーを混合して４０～４００℃における熱膨張係数を８～２５ｐｐｍ／℃に、ヤング率を３０ＧＰａ以下に規定した封止剤により前記半導体素子とボンディングワイヤとを封止せしめた半導体素子実装用配線基板。

【請求項２】請求項１の半導体素子実装用配線基板を外部電極回路基板上に設けた配線基板実装構造。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は半導体素子実装用配線基板に関し、とくに表面実装型の配線基板上にボンディングワイヤを用いて半導体素子を接続した後、半導体素子とボンディングワイヤとを熱硬化性樹脂からなる封止剤を用いて封止し接着せしめた熱履歴特性、耐久性および信頼性に優れた半導体素子実装用配線基板に関するものである。さらにかかる本発明の半導体素子実装配線基板を外部電極回路基板上に設けた配線基板実装構造に関するものである。

【０００２】

【従来の技術】配線基板は絶縁基板の表面あるいは内部にメタライズ配線層を配設したものであって、代表例として半導体素子、とくにＬＳＩ（大規模集積回路素子）等の半導体集積回路素子を載置するための半導体素子収納用パッケージがある。

【０００３】この半導体素子収納用パッケージ（以下、半導体素子収納用パッケージをパッケージと略記する）によれば、アルミナセラミックスからなる絶縁基板の表面および内部に、タングステンやモリブデン等の高融点金属粉末からなる複数個のメタライズ配線層を配設したものであって、絶縁基板の上面に載置した半導体素子に対しワイヤを介して電気的に接続する、いわゆるワイヤボンディング方式が採用される。さらに熱硬化性樹脂からなる封止剤により半導体素子とボンディングワイヤとを封止している。

【０００４】このような構造のパッケージによれば、半導体素子の集積度が高くなると、半導体素子に形成される電極数が増大し、これに伴って配線基板における端子数も増大する。

【０００５】

【発明が解決しようとする課題】上記パッケージを外部電極回路基板上に実装するための半導体素子実装用配線基板として使用する場合、配線基板の接続端子と外部電極回路基板の配線導体とを電気的に接続するが、通常、外部電極回路基板は樹脂成分を含有する有機質材料または有機質材料と無機質材料との複合材で構成されたプリント基板などで構成する。他方、パッケージの絶縁基板はアルミナ、ムライトなどのセラミックスにより構成し、２００ＭＰａ以上の高強度を有し、しかも、メタライズ配線層などの多層化技術を使用することで高い信頼性が得られる。

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【０００６】このような構成の半導体素子実装用配線基板においては、半導体素子の作動時に発する熱が絶縁基板と外部電気回路基板の双方に対し繰り返し印加され、これにより、接続部間に熱応力による歪みが発生していた。ちなみに、絶縁基板と外部電気回路基板の熱膨張係数差は１０ｐｐｍ／℃以上である。

【０００７】パッケージに設けた接続端子が３００個未満程度に比較的少ない場合には、熱応力による影響が小さいが、接続端子が３００個以上になる程度まで大型になると、熱応力も増大し、そのため、半導体素子の作動／停止のサイクルによりパッケージの接続端子の外周部ならびにこの接続端子と外部電気回路基板の配線導体との接合界面に応力が集中し、接続端子が絶縁基板より剥離したり、接続端子が外部電気回路基板の配線導体から剥離し、その結果、パッケージの接続端子を外部電極回路の配線導体に長期にわたり安定して電気的接続できないという課題があった。

【０００８】かかる課題を解消するため、パッケージの絶縁基板の構成材にアルミナ、ムライトなどのセラミックスに代えて、より熱膨張率の大きい高熱膨張率ガラスセラミックス等を用いることが検討されている（特開平８－２７９５７４号、特開平１０－１６７８２２号参照）。

【０００９】この高熱膨張率ガラスセラミックスは熱膨張係数が８～２５ｐｐｍ／℃であり、アルミナセラミックスと比べて相当に高く、パッケージと外部電気回路基板との間の接続部との間に生ずる接続不良が回避できたが、その反面、このような高熱膨張率ガラスセラミックスを用いることで、シリコンからなる半導体素子（熱膨張係数：２～３ｐｐｍ／℃）との熱膨張差が大きくなり、これにより、配線基板のメタライズ配線層と半導体素子の接続用電極とをボンディングワイヤを用いて接続し、さらに半導体素子とボンディングワイヤとを熱硬化性樹脂を含む封止剤を用いて封止してなるパッケージ（絶縁基板）を外部電極回路基板に実装した場合、封止剤と半導体素子の上面コーナー部との間に応力が集中し、封止剤にクラックが発生し、十分な封止ができず、その結果、高温高湿試験等の信頼性試験において接続抵抗が劣化する（電気抵抗が高くなる）という課題が生じた。

【００１０】したがって、本発明者らは上記事情に鑑みて、絶縁基板、半導体素子および封止剤に生じる熱応力を緩和させるべく鋭意研究を重ねた結果、熱膨張係数が８～２５ｐｐｍ／℃に規定された絶縁基板に対し、硬化

後の熱膨張係数（４０～４００℃）が８～２５ｐｐｍ／℃に、ヤング率（４０～４００℃）が３０ＧＰａ以下に規定されるような材料組成の封止剤を被覆することで、かかる熱応力が吸収され、その影響が顕著に小さくなることを見出した。

【００１１】本発明は上記知見により完成されたものであり、その目的はパッケージ等の配線基板およびに半導体素子に被覆した封止剤にクラックが発生しないことで、十分な封止性能を達成し、接続における通電性を高めた半導体素子実装用配線基板を提供することにある。

【００１２】本発明の他の目的はパッケージ等の配線基板を外部電気回路基板に表面実装した際し、長期間にわたって強固にかつ安定して接続させ、これによって長期信頼性を達成した配線基板実装構造を提供することにある。

【００１３】

【課題を解決するための手段】本発明の半導体素子実装用配線基板は、４０～４００℃における熱膨張係数が８～２５ｐｐｍ／℃に規定された絶縁基板の表面および内部にメタライズ配線層を配設してなる配線基板上に、半導体素子を載置し、この配線基板のメタライズ配線層および半導体素子の接続用電極とをボンディングワイヤを用いて接続し、熱硬化性樹脂にフィラーを混合して４０～４００℃における熱膨張係数を８～２５ｐｐｍ／℃に、ヤング率を３０ＧＰａ以下に規定した封止剤により半導体素子とボンディングワイヤとを封止せしめたことを特徴とする。

【００１４】本発明の配線基板実装構造は、かかる本発明の半導体素子実装用配線基板を外部電極回路基板上に設けたことを特徴とする。

【００１５】

【発明の実施の形態】以下、本発明を図により詳細に説明する。図１は前記配線基板であるＢＧＡ型半導体素子収納用パッケージＡ（以下、パッケージＡ）に半導体素子を実装した半導体素子実装用配線基板Ｐの断面図である。図２は半導体素子実装用配線基板Ｐを外部電気回路基板Ｂ（以下、回路基板Ｂ）に実装した配線基板実装構造Ｓの断面図である。

【００１６】図１に示すように半導体素子実装用配線基板ＰはパッケージＡに半導体素子Ｃを実装したものであって、このパッケージＡにおいて、絶縁基板１の表面には半導体素子Ｃと接続されるメタライズ配線層２が形成され、接続パッド３が取り付けられている。メタライズ配線層２はビアホール導体４を通して接続パッド３に電気的に接続されている。

【００１７】半導体素子Ｃはシリコン（Ｓｉ）材料からなり、たとえば熱硬化性樹脂からなる接着層６でもって絶縁基板１の表面に接着固定されている。この熱硬化性樹脂にノボラック型エポキシ樹脂やビスフェノールＡ型エポキシ樹脂を使用すると、絶縁基板１との接着性に優れる点でよい。また、半導体素子Ｃには接続用電極７が設けられ、ボンディングワイヤ８によってメタライズ配線層２と電気的に接続されている。さらに半導体素子Ｃおよびボンディングワイヤ８を封止剤９でもって封止させる。

【００１８】パッケージＡに半導体素子Ｃを実装するには絶縁基板１表面にダイ付け樹脂を塗布した後、半導体素子Ｃを載置し、約１００～２００℃の温度で硬化させ、さらに半導体素子Ｃと絶縁基板１上のメタライズ配線層２をボンディングワイヤ８で接続し、半導体素子Ｃとボンディングワイヤ８とを熱硬化性樹脂でもって被覆し封止した後、約１００～２００℃の温度で硬化させ、封止剤９となす。

【００１９】図２に示すように上記構成の半導体素子実装用配線基板Ｐを接続端子５を介して回路基板Ｂに実装して配線基板実装構造Ｓとする。接続端子５はボール状の半田ボールにより構成され、接続パッド３に対して半田等により取着されている。

【００２０】回路基板Ｂは絶縁基体１０を主体とし、絶縁基体１０はエポキシ樹脂、フェノール樹脂、アラミド樹脂、ポリイミド樹脂、ポリオレフィン樹脂から選ばれる少なくとも１種の熱硬化性樹脂に対し、フィラー成分としてガラスなどを含むガラス－エポキシ樹脂、ガラス－ポリイミド樹脂複合材料などからなる。この絶縁基体１０の表面にＣｕ、Ａｕ、Ａｌ、Ｎｉ、Ｐｂ－Ｓｎから選ばれた少なくとも１種の金属を含む配線層１１が被着形成されたものであって、プリント基板などに相当する。

【００２１】つぎに絶縁基板１と封止剤９を詳述する。

絶縁基板１

４０～４００℃における熱膨張係数が８～２５ｐｐｍ／℃に規定されるようにセラミックスから材料選択するとよく、望ましくは４０～４００℃でのヤング率が２００ＧＰａ以下、好適には１５０ＧＰａ以下のセラミックス材により構成する。

【００２２】このような特性の材料として、たとえば特開平１０－１６７８２２号の明細書中に記載されているようなリチウム珪酸系ガラス、ＰｂＯ系ガラス、ＺｎＯ系ガラス、ＢａＯ系ガラス等のガラス成分に対し、エンステタイト、フォルステライト、SiO_2 系フィラー、ＭｇＯ、ZrO_2 、ペタライト等の各種セラミックフィラーを混合し、ついで焼成したものがある。

【００２３】これらセラミックフィラーのうち、好適にはＢａＯを５～４０重量％含有するガラスを２０～８０体積％の割合で、クォーツを８０～２０体積％の割合で含有する成形体を焼成して得られた焼結体がよい。さらに好適には焼結体の耐薬品性の観点からクォーツの一部をジルコニアに置換して得られた焼結体が望ましい。

【００２４】この焼結体であれば、均質の製品を良好な再現性でもって容易に製造することができ、加えてガラ

ス成分にＢａＯを５～４０重量％含有することで、屈伏点が比較的低くなり、これにより、ガラス成分の添加量が少なくても低温焼成ができ、その結果、Ｃｕ、Ａｇ等からなるメタライズ配線層と同時に焼成することができる。

【００２５】さらにＢａＯ系ガラスの屈伏点が４００～８００℃にまで低くなることで、ガラス含有量が低減でき、これに伴いフィラー量を増加でき、しかも、焼成収縮開始温度を上げることもできるので、成形時に添加された有機樹脂等の成形用バインダーを効率的に除去でき、絶縁体と同時焼成されるメタライズ層との焼成条件をマッチングできる。このようにＢａＯ系ガラスの屈伏点を規定する場合、その屈伏点が４００～６５０℃の範囲内になるような組成にするとよい。

【００２６】封止剤９

封止剤９は熱硬化性樹脂にフィラーを混合したものであって、その混合状態を調整して、硬化後において４０～４００℃における熱膨張係数が８～２５ｐｐｍ／℃に、ヤング率が３０ＧＰａ以下になるのであれば、さまざまな組成がある。

【００２７】この熱硬化性樹脂には、たとえばフェノール樹脂、ユリア樹脂、メラミン樹脂、エポキシ樹脂、不飽和ポリエステル樹脂、フタル酸ジアリル樹脂、ポリイミド樹脂、シリコーン樹脂、ポリウレタン樹脂などがあり、就中、ビスフェノール系エポキシ樹脂、フェノールノボラック系エポキシ樹脂、クレゾールノボラック系エポキシ樹脂、ブロム化エポキシ樹脂、脂環式エポキシ樹脂などのエポキシ樹脂が好ましい。

また、封止剤のヤング率および熱膨張係数を前記の範囲に制御するためには、熱硬化性樹脂に対して、石英ガラス、アルミナ、マイカ、ジルコニウムシリカケート、リチウムシリケート等の無機質を前記熱硬化性樹脂１００重量部に対して、１００～１５０重量部でもって配合して調整する。

【００２８】このように組成を調整することで、熱硬化性樹脂が硬化した後での封止剤９の熱膨張係数を８～２５ｐｐｍ／℃に、かつヤング率を３０ＧＰａ以下にする。

【００２９】熱膨張係数が８ｐｐｍ／℃未満になると、フィラー量が多くなり、そのために樹脂の流動性が低くなり、実装効率が低下し、さらに絶縁基板１に対する接着力が低下する。また、２５ｐｐｍ／℃を超えると高温時と低温時との間での熱膨張および熱収縮の差が大きくなり、封止剤９と半導体素子Ｃの上面コーナー部との間に応力が集中し、封止剤９にクラックが発生する。望ましくは熱膨張係数を８～２０ｐｐｍ／℃にするとよい。

【００３０】また、封止剤９のヤング率は３０ＧＰａ以下に、好適には２５ＧＰａ以下にするとよく、ヤング率が３０ＧＰａを超えると変形量が小さく、封止剤９と半導体素子Ｃの上面コーナー部との間に応力が集中し、封止剤９にクラックが発生する。

【００３１】かくして本発明の半導体素子実装用配線基板Ｐによれば、絶縁基板１の熱膨張係数を８～２５ｐｐｍ／℃（４０～４００℃）に、望ましくはヤング率を２００ＧＰａ以下（４０～４００℃）に規定するとともに、封止剤９の熱膨張係数を８～２５ｐｐｍ／℃（４０～４００℃）に、ヤング率を３０ＧＰａ以下に規定することで、半導体素子Ｃなどに起因する熱応力が絶縁基板１のたわみにより吸収されるとともに、絶縁基板１と封止剤９の熱硬化性樹脂（ポッティング樹脂）との双方の熱膨張係数を近づけることで、基板に反りが発生することがなく、回路基板Ｂとの接続部に発生する応力を低減でき、封止剤９と半導体素子Ｃの上面コーナー部との間に発生する応力の集中が回避され、その結果、封止剤９にクラックが発生しなくなり、半導体素子ＣおよびボンディングワイヤＢが保護され、長期使用に対し高い信頼性が達成される。

【００３２】

【実施例】表１に示すとおり３種類のセラミックス（絶縁基板材Ａ、Ｂ、Ｃ）を用意し、各々のセラミックス材料でもって５×４×４０mmの形状の焼結体を作製した。

【００３３】

【表１】

絶縁基板材	ガラス成分		フィラー成分	
	組成 （ ）内は重量%	体積%	組成	体積%
A	SiO_2(78)-Li_2O(10)-Al_2O_3(4)-K_2O(4)-P_2O_5(2)-Na_2O(2)	50	フォルステライト	50
B	SiO_2(78)-Li_2O(10)-Al_2O_3(4)-K_2O(4)-P_2O_5(2)-Na_2O(2)	35	フォルステライト クオーツ	30 35
C	SiO_2(45)-Al_2O_3(6)-B_2O_3(9)-CaO(5)-BaO(37)	50	クオーツ	50

【００３４】ついで、各焼結体についてヤング率および４０～４００℃における熱膨張係数を測定したところ、表２に示すような結果が得られた。

【００３５】

【表２】

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絶縁基板材	ヤング率 (GPa)	熱膨張係数 (ppm/℃)
A	１０８	１１．７
B	１１４	１４．６
C	８０	１２．２

【００３６】また、各絶縁基板材Ａ、Ｂ、Ｃを用いて、厚み０．４ｍｍの絶縁基板１を作製した。その際、銅を主成分とするメタライズ配線層およびスルーホールを形成し、基板上面のスルーホールと接続する箇所には多数のＣｕメタライズからなる接続パッドを形成した。

【００３７】ついで、Ｓｉからなる半導体素子Ｃ（４０～４００℃における熱膨張係数：２．６ｐｐｍ／℃）をダイ付け樹脂を用いて１５０℃で１時間大気中で接着した。その後、半導体素子Ｃと絶縁基板１上のメタライズ配線層２をボンディングワイヤ８で接続した。

【００３８】しかる後、絶縁基板材Ａ、Ｂ、Ｃからなる各種絶縁基板１において、さらに半導体素子Ｃとボンディングワイヤ８の上に表３および表４に示すような各種封止材を被覆し、１８０℃の加熱温度でもって２時間大気中にて硬化させ、試料Ｎｏ．１～試料Ｎｏ．２４の各種半導体素子実装用配線基板Ｐを作製した。

【００３９】これらの表にて示すように、封止材の熱硬化型樹脂としてフェノールノボラック型エポキシ樹脂やクレゾールノボラック型エポキシ樹脂を使用し、それにフィラーとして石英ガラスやアルミナを添加し、そして、混練し調製したものを用いた。

【００４０】

【表３】

試料 Ｎｏ	絶縁基板材料	封止剤の組成	
		樹脂の種類	石英ガラス (重量部)
1	A	フェノールノボラック型エポキシ樹脂	５０
2			１００
3			１１０
4			１３０
5			１５０
6			２００
7	B	クレゾールノボラック型エポキシ樹脂	５０
8			１００
9			１１０
10			１３０
11			１５０
12			２００

【００４１】

【表４】

8

試料 Ｎｏ	絶縁基板材料	封止剤の組成	
		樹脂の種類	アルミナ (重量部)
13	C	フェノールノボラック型エポキシ樹脂	５０
14			１００
15			１１０
16			１３０
17			１５０
18			２００
19	A	クレゾールノボラック型エポキシ樹脂	５０
20			１００
21			１１０
22			１３０
23			１５０
24			２００

【００４２】また、これら半導体素子実装用配線基板Ｐに使用する封止材の熱膨張係数およびヤング率を表５と表６に示す。

【００４３】

【表５】

試料 Ｎｏ	熱膨張係数 (ppm/℃)	ヤング率 (GPa)	ＴＣＴ (回)
1	６２	８．６	８００
2	３５	１５．４	９００
3	３２	１６．６	９５０
4	２５	２１．４	＞１０００
5	１８	２７．４	＞１０００
6	１２	３３．４	９００
7	４３	７．２	９００
8	３２	９．３	９２５
9	３０	２０．５	９５０
10	２０	２４．５	＞１０００
11	８	２９．７	＞１０００
12	４	３４．９	９００

【００４４】

【表６】

9

試料No	熱膨張係数(ppm/℃)	ヤング率(GPa)	TCT(回)
13	63	9.1	850
14	47	16.3	900
15	45	17.5	900
16	36	22.4	900
17	25	28.3	>1000
18	13	42.3	850
19	50	13.6	900
20	23	22.5	>1000
21	21	23.4	>1000
22	17	26.8	>1000
23	12	31.3	950
24	7	36.6	900

【００４５】これら熱膨張係数αおよびヤング率Ｅはつぎのように求めた。樹脂を１５０℃、１時間保持し、硬化させ、そして、熱膨張係数αはＴＭＡ法（サンプルサイズ：３．５×３．５×１５mm）で、ヤング率ＥはＤＨＡ法（サンプルサイズ：５×０．５×５０mm）によって求めた。

【００４６】かくして得られた試料Ｎｏ．１～試料Ｎｏ．２４の半導体素子実装用配線基板Ｐについて、熱サイクル試験をおこなったところ、表５と表６に示すような結果が得られた。

【００４７】熱サイクル試験については、－４０℃と１２５℃の各温度に制御した恒温槽中に試験サンプル（半導体素子実装用配線基板Ｐ）をそれぞれ１５分間ずつ保持し、これを１サイクルとし、このサイクルを最高１０００回まで繰り返した。そして、各サイクル毎に半導体素子とボンディングワイヤについて、それぞれの封止剤内での剥がれ状態を確認し、剥がれが発生するまでのサイクル数をカウントした。

【００４８】これらの表より明らかなように、封止剤の熱膨張係数が８～２５ｐｐｍ／℃でヤング率が３０ＧＰａ以下である材料、試料Ｎｏ．４、５、１０、１１、１７、２０～２２では半導体素子とボンディングワイヤとを配線基板上で封止した封止剤の剥がれは、熱サイクル１０００回までまったく見られず、きわめて安定で良好な封止状態を維持できた。上記範囲外の試料No.１～

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３、６～９、１２～１６、１８、１９、２３、２４では１０００サイクル未満で封止剤の剥がれが発生し、実装後の信頼性に欠けることがわかった。

【００４９】

【発明の効果】以上のとおり、本発明の半導体素子実装用配線基板によれば、４０～４００℃における熱膨張係数が８～２５ｐｐｍ／℃に規定された絶縁基板の表面および内部にメタライズ配線層を配設してなる配線基板上に、半導体素子を載置し、さらに熱硬化性樹脂にフィラーを混合して４０～４００℃における熱膨張係数を８～２５ｐｐｍ／℃に、ヤング率を３０ＧＰａ以下に規定した封止剤によって封止したことで、その封止剤にクラックが発生しなくなり、これによって十分な封止性能が達成され、その結果、接続における通電性を高めた半導体素子実装用配線基板が提供できた。

【００５０】また、本発明の配線基板実装構造においては、かかる本発明の半導体素子実装用配線基板を外部電極回路基板上に表面実装したことで、長期間にわたって強固にかつ安定して接続でき、これによって長期信頼性を達成した配線基板実装構造が提供できた。

【図面の簡単な説明】

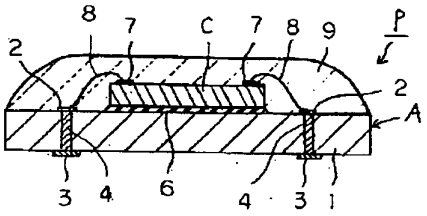
【図１】本発明の半導体素子実装用配線基板の断面図である。

【図２】本発明の配線基板実装構造の断面図である。

【符号の説明】

A	ＢＧＡ型半導体素子収納用パッケージ
B	外部電気回路基板Ｂ
S	配線基板実装構造
P	半導体素子実装用配線基板
C	半導体素子
1	絶縁基板
2	メタライズ配線層
3	接続パッド
4	ビアホール導体
5	接続端子
6	接着層
7	接続用電極
8	ボンディングワイヤ
9	封止剤
１０	絶縁基体
１１	配線層

【図１】



【図２】